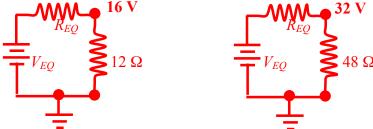
P214 Final Practice Problem **SOLUTIONS**

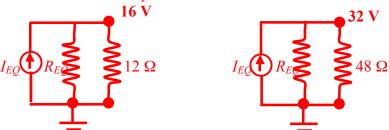
- 1. A sinusoidal waveform is displayed on an oscilloscope and has a peak-to-peak amplitude of 15 V. At the same time, the signal is measured on a multimeter which is set to measure AC voltage. What value would you expect to be displayed on the multimeter? The RMS voltage of a sinusoidal waveform is (the peak voltage)/ $\sqrt{2}$, which is (the peak-to-peak voltage)/ $(2\sqrt{2})$. Thus, the RMS voltage here is $15/(2\sqrt{2}) = 5.3$ volts. Multimeters on AC voltage settings display RMS voltages, thus the multimeter will display **5.3 volts**.
- 2. A pair of terminals is investigated by measuring the output voltage when connected to two different loads. When a resistance of 12 Ω is connected across the output, the output voltage is 16 V, and when a load of 48 Ω is connected, the output voltage is 32 V. Determine the Thevenin and the Norton equivalents of the circuit behind the terminals.

We have the Thevenin equivalent circuits:



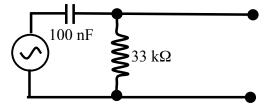
To find V_{EQ} and R_{EQ} , we note that, from the first circuit, $16 = (12V_{EQ})/(12 + R_{EQ})$ (because $I = V_{EQ}/(12 + R_{EQ})$, and thus the voltage across the 12 Ω resistor = 12 $I = (12V_{EQ})/(12 + R_{EQ})$), and from the second circuit, $32 = (48V_{EQ})/(48 + R_{EQ})$. Solving those two equations for V_{EQ} and R_{EQ} , we get $V_{EQ} = 48$ V and $R_{EQ} = 24$ Ω .

We have the Norton equivalent circuits:



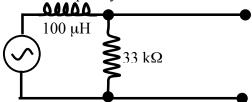
We know that $I_{EQ} = V_{EQ}/R_{EQ} = 2$ A (you can check that that value is consistent with the two circuits above).

3. Calculate the time constant τ and the cut-off angular frequency ω of the following circuit. Is it a high- or low-frequency cut-off?



The time constant $\tau = RC = 33 \times 10^3 \times 100 \times 10^{-9} = 3.3 \times 10^{-3}$ seconds = **3.3 milliseconds**. The cut-off angular frequency $\omega = 1/RC = 1/(3.3 \times 10^{-3}) = 3 \times 10^2$ radians/second. At high frequencies, the capacitor will "look like a wire" and thus this circuit will be a high-pass filter, i.e. a filter that cuts off low frequencies (and passes high ones).

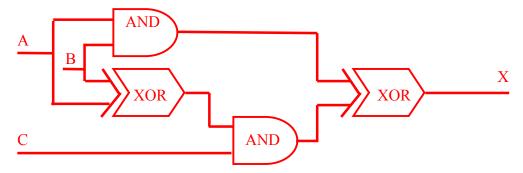
4. Calculate the time constant τ and the cut-off angular frequency ω of the following circuit. Is it a high- or low-frequency cut-off?



The time constant τ of an RL circuit is L/R = $(100 \times 10^{-6})/(33 \times 10^{3}) = 3 \times 10^{-9}$ seconds = 3 nanoseconds. The cut-off angular frequency $\omega = 1/\tau = 1/(3 \times 10^{-9}) = 3.3 \times 10^{8}$ radians/second. At low frequencies, the inductor will "look like a wire" and thus this circuit will be a low-pass filter, i.e. a filter that cuts off high frequencies (and passes low ones).

5. Design a logic circuit to take 3 inputs: A, B, and C, and produce a single output X, such that X is true if, and only if, precisely two of its inputs are true.

There are several options for correct answers to this question; one of them is:

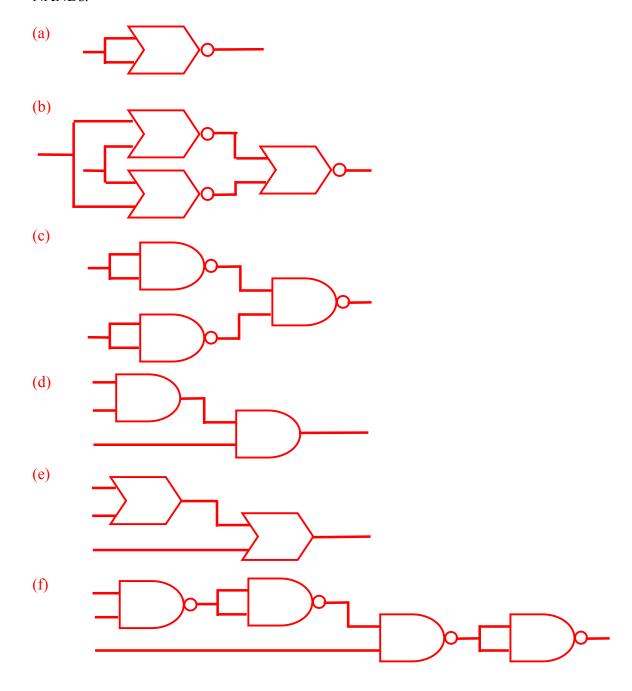


6. Bugg problem 13.9.4

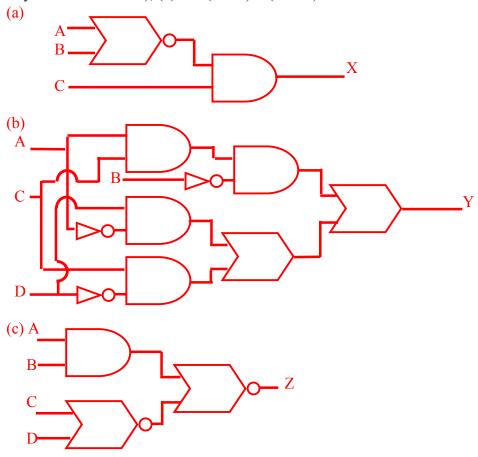
Each of the 3 JK flip-flops will start out with Q = 0, $\overline{Q} = 1$. The clock inputs on each of the JK flip-flops are positive-edge triggered (as there is a triangle but no dot). As a first pulse comes in, it will flip Q on the first flip-flop to 1 and \overline{Q} to 0. When a second pulse comes in, it will flip Q on the first flip-flop back to 0 and \overline{Q} to 1, which will trigger the second flip-flop to flip Q to 1 and \overline{Q} to 0. When a third pulse comes in, it will flip Q on the first flip-flop to 1 and \overline{Q} to 0, so that the outputs of both the first and the second flip-flop are both 1. When a fourth pulse comes in, it will flip Q on the first flip-flop back to 0, \overline{Q} to 1, and thus on the second flip-flop, Q will go back to 0, \overline{Q} will go to 1, which will trigger the third flip-flip to flip Q to 1, and \overline{Q} to 0. Thus, this circuit is acting as a 3-digit binary counter, with the largest digit (the 4's = 2²) being the third flip-flop, the middle digit (the 2's = 2¹) being the middle flip-flop, and the smallest digit (the 1's = 2⁰) being the first flip-flop. The waveforms will be as drawn in Fig. 13.26, but with the important change that the +2 and +4 outputs should actually have their changes occur at the *rising* edge of each second and each fourth pulse respectively, not on the falling edge. If Bugg had meant

that the changes should occur on the falling edges of the pulses, then he should have drawn inverting bubbles on the front of each of the clock inputs to the 3 flip-flops...

7. Using 2-input gates, show how to make (a) a NOT inverter from a NOR gate, (b) an OR gate from NOR gates, and (c) an OR gate from NAND gates. Also show how to make (d) a 3-input AND from 2-input ANDs, (e) a 3-input OR from 2-input ORs, and (f) a 3-input AND from 2-input NANDs.



8. Implement the following expressions using standard logic gates, and draw the resulting circuits: (a) $X = (\overline{A} + \overline{B}) \cdot C$, (b) $Y = A\overline{B}C + \overline{A}D + C\overline{D}$ (dots are omitted in the ANDs in this expression, as you see sometimes), (c) $Z = (\overline{A} \cdot \overline{B}) + (\overline{C} + \overline{D})$.



9. Switch bounce is an issue you sometimes see with electro-mechanical switches – when the switch is switched, for a millisecond or two there will be oscillations where the switch loses contact (before the switch settles down after a couple of milliseconds). Design a sequential logic circuit using two input NOR gates to remove the effects of switch bounce from an electro-mechanical logic switch.

The answer to this is in the paragraph entitled "Debounce circuit" on the middle of page 258 in the Bugg textbook.

10. Essentially all the Bugg problems that we didn't have as homework, but are in the Bugg chapters that we did cover, would be good practice problems for the final. (And the ones that you did have as homework are of course good too, but you've already done those as homework.)

Ask me questions, e.g. at the review session, if you have questions on any of these.